REMARKS

Claims 1-41 are currently pending. Claims 1, 6, 11, 19, 29, and 33 have been amended without acquiescence in the Office Action's basis for neither rejections nor prejudice to pursue in a related application. No new matter has been added.

Rejections Under 35 U.S.C. § 102

Claims 1-41 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al., U.S. Patent No. 6,430,731 (hereinafter "Lee"). Applicant respectfully traverses.

Independent claim 1 recites the following features:

> selecting, by using a processor, one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least in part upon the timing model, wherein the timing model comprises a load data of the gate, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews of the plurality of timing events such that the one of the plurality of timing events propagated to the input of the gate with a worst output slew as a function of input slew is selected as the worst case timing event (emphasis added).

Applicant respectfully submits that Lee fails to disclose each and every feature of the present claims in a manner as recited therein. For example, Lee does not select any timing event propagated to the input of the gate, with the worst output slew as a function of input slew, as the worst case timing event.

Lee merely discloses a calculated representative signal. The ***representative*** signal (s_j, a_j) of Lee is ***computed*** with the arrival time and slew at the input pin according to equation (26). As clearly disclosed by Lee, Lee uses only slew at the input pin (s_j) and arrival time (a_j). Lee's equation only considers slew at the input pin (s_j) and arrival time (a_j) for calculated boundary signals and not selecting the worst timing event propagated to the input of the gate using the worst output slew. Lee is completely silent with respect to using the worst output slew to select any timing events.

In addition, the computed signal is not the worst propagated timing event because the calculated representative signals are used for boundary signals. Merely calculating the representative signal does not disclose or suggest a timing event propagated to the input of the gate as the worst case timing event having the worst output slew as a function of input slew. A

representative signal or boundary signals for the circuit are not the same as a timing event propagated to the input of the gate because the representative signal is a signal calculated and not a signal propagated to the input. Thus, Lee ***calculates*** a representative signal with arrival time and slew, which is not the same as selecting the worst case timing event propagated to the input of the gate having the worst output slew as a function of input slew as claimed.

Moreover, mere mentioning of capacitance loading in Lee does not explicitly or implicitly disclose that the signal in Lee is calculated based on any load data. In fact, Lee clearly teaches away from the claims. As stated in column 4, lines 32-33 and 47-49 of Lee, Lee explicitly shows that it is not desirable to use capacitance loading in calculating the signal of Lee. Those lines disclose that it is not desirable to use load data because they are irrelevant to Lee's invention such as calculating the signal. As disclosed in Lee, for each input pin to output pin path inside a gate, the signal arrival time and slew at the output pin are functions of the signal arrival time, slew at the input pin and other circuit parameters such as capacitance loading. The dependence on the other circuit parameters was dropped by Lee for clarity as it is irrelevant to an understanding of the present invention of Lee. Thus, Lee's representative signal calculation does not consider capacitance loading because, even though capacitance loading may be considered along with the slew and arrival time, Lee concluded that capacitance loading information is irrelevant and not desirable in calculating the signal of Lee's invention. Thus, Lee teaches away from the claims by calculating the signal using only the signal arrival time and slew, and not the irrelevant other parameters such as load data.

Therefore, Lee explicitly teach away from the claimed invention by disclosing calculating a signal without using capacitance loading information as Lee believes that information to be irrelevant. This is further shown by the equations of Lee where load data is never part of those equations.

Thus, Lee does not disclose "selecting, by using a processor, one of the plurality of timing events propagated to the input of the gate as a worst case timing event based at least in part upon the timing model, wherein the timing model comprises a load data of the gate, an arrival time in the plurality of different arrival times and a slew in the plurality of different slews of the plurality of timing events such that the one of the plurality of timing events propagated to the input of the gate with a worst output slew as a function of input slew is selected as the worst

case timing event" (emphasis added). For at least these reasons, it is respectfully submitted that independent claim 1 is not anticipated by the Lee reference.

For at least these same reasons, it is respectfully submitted that independent claims 6, 11, 19, 29 and 33 are likewise not anticipated by the cited references because they recite a limitation substantially similar to the limitation identified discussed with respect to claim 1 .

Since the remaining claims depend from these independent claims 1, 6, 11, 19, 29 and 33, respectively, these remaining dependent claims are also not anticipated and are therefore allowable over the cited references for the same reasons discussed above with respect to claim 1.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

While rendered moot by the above reasons, the Applicant notes and formally states that to the extent there are any suggestions or statements of admissions of prior art or judicial notice of art by the Office Action, those implications of admission by Applicant or judicial notice by the Office Action are hereby traversed.

To the extent that any arguments and disclaimers were presented to distinguish prior art, or for other reasons substantially related to patentability, during the prosecution of any and all parent and related application(s)/patent(s), Applicant(s) hereby explicitly retracts and rescinds any and all such arguments and disclaimers, and respectfully requests that the Examiner re-visit the prior art that such arguments and disclaimers were made to avoid.

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Respectfully submitted,

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